Claims: Cancel the claims 1 to 20 of record:

1.-20. (Canceled)

Substitute new claims 21 to 38 as follows:

21. (New) An automatic gain control circuit comprising:

an amplifier having at least a received signal and an analog gain control signal as separate inputs, wherein said amplifier amplifies said received signal by an amplification factor to generate an amplified analog signal;

an analog-to-digital converter configured to convert said amplified analog signal into an amplified digital signal;

a signal strength estimator configured to measure signal strength of said amplified digital signal;

a gain adjusting factor device configured to generate a gain adjusting factor;

a multiplier configured to multiply a digital gain control signal by said gain adjusting factor; and

a digital-to-analog converter configured to convert the digital gain control signal into said analog gain control signal,

whereby said gain adjusting factor device generates said gain adjusting factor according to said signal strength, and

whereby said analog gain control signal determines said amplification factor.

22. (New) The automatic gain control circuit according to claim **21**, further comprising:

a mapping device configured to map a signal into a different signal; and

a delay device configured to insert predefined delay for a loop.

23. (New) The automatic gain control circuit according to claim **21**, wherein said gain adjusting factor device comprises means for generating the gain adjusting factor based on a predetermined relation between the signal strength and a reference gain adjusting factor.

24. (New) The automatic gain control circuit according to claim **23**, wherein said predetermined relation is described by one from a group consisting of a mathematical formula, a curve, and a set of number pairs.

25. (New) The automatic gain control circuit according to claim **21**, wherein said gain adjusting factor device comprises means for generating the gain adjusting factor inversely proportional to said signal strength.

26. (New) The automatic gain control circuit according to claim **21**, wherein said gain adjusting factor device has signal strength, a plurality of reference signal strengths, and a plurality of reference gain adjusting factors as input and the gain adjusting factor as its output.

27. (New) The adjusting factor device according to claim **26**, further comprising:

a comparing logic circuit configured to generate an index according to the measured signal strength; and

a selecting logic circuit configured to select the gain adjusting factor from the plurality of reference gain adjusting factors according to said index.

28. (New) An automatic gain control circuit, comprising:

an amplifier having at least a received signal and an analog gain control signal as separate inputs, wherein said amplifier amplifies said received signal by an amplification factor controlled by said analog gain control signal to generate an amplified analog signal;

an analog-to-digital converter, coupled to output of said amplifier, for converting said amplified analog signal into an amplified digital signal;

a signal strength estimator, coupled to output of said analog-to-digital converter, for measuring signal strength of said amplified digital signal;

a first memory device, coupled to output of said signal strength estimator, for storing a plurality of samples of said signal strength;

a gain generating device, coupled to output of said first memory device, for generating a digital gain control signal; and

a digital-to-analog converter configured to convert the digital gain control signal into said analog gain control signal,

whereby said gain generating device comprises means to generate said digital gain control signal according to said plurality of samples of said signal strength.

29. (New) The automatic gain control circuit according to claim 28, further comprising:

a delay device configured to insert a predefined delay into a loop consisting of said amplifier, said analog-to-digital converter, said signal strength estimator, said gain generating device, and said digital-to-analog converter to produce a delayed digital gain control signal; and

a second memory device configured to store a plurality of samples of said digital gain control signal.

30. (New) The automatic gain control circuit according to claim 29, wherein said means to generate said digital gain control signal is based on a predefined relation of a new digital gain versus current sample of said digital gain control signal, current sample of said signal strength, and a plurality of previous samples of said signal strength.

31. (New) The automatic gain control circuit according to claim 28, wherein said means to generate said digital gain control signal is based on a predefined relation of a new digital gain versus current sample of said digital control gain signal, current sample of said signal strength, and a plurality of previous samples of said signal strength.

32. (New) The automatic gain control circuit according to claim 29, wherein said gain generating device comprising means for updating the digital gain control signal based on the samples of said signal strength stored on said first memory device and the samples of said digital gain control signal stored on said second memory device.

33. (New) The automatic gain control circuit according to claim 28, wherein said gain generating device comprises means for generating said digital gain control signal dynamically by making use of other information and following a predefined gain adjusting procedure.

34. (New) The automatic gain control circuit according to claim 29, wherein said gain generating device comprises means for generating the digital gain control signal differently under different scenarios.

35. (New) A method for automatically varying a gain control signal for a receiver, comprising the steps of: